

Abstract of the Disclosure

A non-volatile memory device comprises a cell region defined at a substrate and a plurality of device isolation layers formed in the cell region to define a plurality of active regions. A charge storage insulator covers substantially the entire top
5 surface of the cell region. A plurality of gate lines are formed on the charge storage insulator that cross over the device isolation layers. Conductive patterns are disposed between predetermined gate lines that penetrate the charge storage insulator to electrically connect with the active regions. According to the method of fabricating the device, a plurality of device isolation layers are formed in the substrate and then a
10 charge storage insulator is formed on an entire surface of the substrate and the device isolation layers. A plurality of parallel gate lines that cross over the device isolation layers are formed on the charge storage insulator and then conductive patterns are formed between predetermined gate lines. The conductive patterns penetrate the charge storage insulator and electrically connect with the active regions.